References

Svoboda, Antonin. "Class Notes In Engineering 125A," Computer Science Department, School of Engineering and Applied Science, University of California, Los Angeles, 1966 and 1972•

_____. "Proposal for Research in Automated Design of-Switching Circuits," UCLA-P-1482-N, May 1967.

_____. "Ordering of Implicants," IEEE Trans., EC-16(2):100-105, Feb. 1967.

_____. "Synthesis of Logical Systems of a Given-Activity," IEEE Trans., EC-12(12):904-910, Dec. 1963 .

_____. "Boolean Analyzer," Information Processing 68. North Holland, Amsterdam, 1969, pp. 824-830.

_____. "Parallel Processing in Boolean Algebra," IEEE Trans., C-22(9):848-851, Sept. 1973.

_____. "Boolean Analyzer Solutions of Fundamental Logic-Design Problems," 1974 (unpublished).

_____. "Logical Systems and Spaces," Paper Distributed at the Symposium on Computers, Prague, Czechoslovakia, 1964.

_____. "Some Applications of Contact Grids," Proceedings, International Symposium.on the Theory of Switching,·Harvard U. Press, Cambridge, Mass., 1959, pp. 293-305.

_____. "Logical Instruments for Teaching Logical Design," IEEE Trans. on Educ., E-12(4):262-273, Dec. 1969.

_____. "The Concept of Term Exclusiveness and Its Effect on the Theory of Boolean Functions," JACM, 22(3):425-440, July 1975.

DeVries, Ronald C., and Antonin Svoboda. "Multiple-Output Optimization with Mosaics of Boolean Functions, IEEE Trans., C-24(8):777-785, Aug. 1975.

Marquand, Allan. "On Logical Diagrams for n Terms," Philosophical Magazine, V. 12, pp. 266-270, 1881 (year). *[Marquand Mapping]*

Karnough, M. "The Map Method for Synthesis of Combinational Logic Circuits," AIEE, pp. 593-599, Nov. 1953. *[Karnough Maps]*

Bearnson, L. W. and C. C. Carroll. "On the Design of Minimal Length Fault Tests for Combinational Circuits," IEEE Trans., C-20(11):1353-1356, Nov 1971.

Bouricius, W. G., et al. "Algorithms for Detection of Faults on Logic Circuits," Digest of Papers of the 1971 International Symposium on Fault Tolerant Computing, Pasadena, CA, March 1971 (IEEE pub # 71-C-6-C), pp. 5-8.

Kohavi, Zvi, and DeWayne Spires. "Designing Sets of Fault Detection Tests for Combinational Logic Circuits," IEEE Trans., C-20(12):1463-1469, Dec. 1971.

Kohavi, lgal and Zvi Kohavi. "Detection of Multiple Faults in Combinational Logic Networks," IEEE Trans., C-21(6):556-568, June 1972.

Marin, Miguel A. "Investigation of the Field of Problems for the Boolean Analyzer," Computer Science Department, University of California, Los Angeles, UCLA-ENG-6828, June 1968 (PhD Thesis).

White, D. E. "Fau1t Detection Through Para11e1 Processing in Boolean Algebra," UCLA-ENG-7504, March 1975 (PhD·Thesis).

_____ "Test Sequence Alternative to Fault Detection," Seminar notes presented at Cal. State Polytechnic Institute, October 1974.

White, D. E., and Antonin Svoboda. "Fault Detection in Combinational Circuits: The Test Sequence," Proceedings, The Eighth Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA., Dec. 1974. pages UKN.

McCluskey, E. J. "Minimization of Boolean Functions," Bell Syst. Tech. J., 35:1417-1444, 1956.

Marinos, Peter N. "Derivation of Minimal Complete Sets of Test Input Sequences Using Boolean Differences," IEEE Trans., C-20(1):25-32, Jan. 1971.

Sellers, F. F., M. Y. Hsiao, and L. W. Bearnson. "Analyzing Errors with the Boolean Difference," IEEE Trans., C-17(4) :676-683 , July 1968 , Correction, C-18(4):381, April 1969.

Yau, Stephen S., and Yu-Shan Tang. "An Efficient Algorithm for Generating Complete Test Sets for Combinational Logic Circuits," IEEE Trans., C-20(11):1245-1251, Nov. 1971.

Armstrong, D. B. "On Finding a Nearly Minimal Set of Fault Detection Tests for Combinational Logic Nets," IEEE Trans., EC-15(2):66-73, Feb. 1966.

Hsiao, M. Y., and Dennis K. Chia. "Boolean Difference for Fault Detection in Asynchronous Sequential Machines," IEEE Trans., C-20 (11):1356-1361, Nov. 1971

Friedman, Arthur D., and P. R. Menon, Franklin F. Kho, ed. Fault Detection in Digital Circuits. Computer Applications in Electrical Engineering Series, Prentice-Hall, Englewood Cliffs, New Jersey, 1971.

Friedman, Arthur D. "Fault Detection in Redundant Circuits," IEEE·Trans., C-16(2):99-100, Feb. 1967.

_____ "Diagnosis of Short Circuit Faults in Combinational Circuits," IEEE Trans., C-23(7):746-752, July 1984.

Avizienis, Algirard. "Fault Tolerant Computers: Theory and Design of Ultra Reliable (Fault Tolerant) Computers: Protective Redundancy, Diagnosis, Self Repair Techniques," Class Notes, UCLA Seminar ENG 298/ENG 867.7, March 1971.

Howell, T. H. Design Criteria for Error Detecting and Error Correcting Codes in Memory Subsystems, (February 1972 PhD Thesis) to be published by Garland.

Basham, Gary R. " New Error Correcting Technique for Solid State Memories Saves Hardware," Computer Design, pp. 110-113, Oct. 1976.

Berger, Isreal, and Zvi Kohavi. "Fault Detection in Fan-Out Free Combinational Networks," IEEE Trans., C-22(10):908-914, October 1973.

White, D. E., et al. Introduction to Designing with the Am2900 Family [Bit-Slice Microprogrammed Control Devices]," Class Notes for A.MD, Inc. Seminar ED2900A, June 1978.

Muroga, Sabure, and Hung Chi Lai. "Minimization of Logic Networks Under a Generalized Cost Function," IEEE Trans., C-25(9):893-907, Sept. 1976.